



The diagram illustrates a 10-layer PCB cross-section. The layers are labeled as follows from top to bottom:

- LAYER 1 (TOP SIDE)**: Solid white layer.
- LAYER 2 (SIGNAL LAYER)**: Hatched layer.
- LAYER 3 (GROUND PLANE)**: Solid white layer.
- LAYER 4 (SIGNAL LAYER)**: Hatched layer.
- LAYER 5 (SIGNAL LAYER)**: Solid white layer.
- LAYER 6 (VOLTAGE PLANE)**: Hatched layer.
- LAYER 7 (SIGNAL LAYER)**: Solid white layer.
- LAYER 8 (BOTTOM SIDE)**: Solid white layer.

External features and dimensions include:

- SILKSCREEN (TOP SIDE)** and **SOLDERMASK (TOP SIDE)** at the top.
- SOLDERMASK (BOTTOM SIDE)** and **SILKSCREEN (BOTTOM SIDE)** at the bottom.
- A vertical dimension line indicates a thickness of **.062 +/- .007** for the central core.
- Reference numbers **11)** and **12)** are shown on the right side.
- The text **LAY 8** is partially visible on the right side.

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PROJ MGR:	ARTEC DG							
CLIENT: ZF Linux Devices, Inc.		SIZE B	DRAWING NUMBER 9400-0048-03-X3		SCALE 1 : 1	SHEET 2 OF 2	REVISION 3	

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