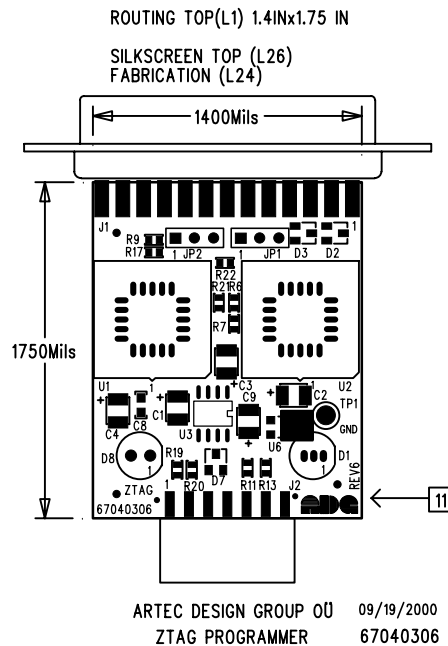


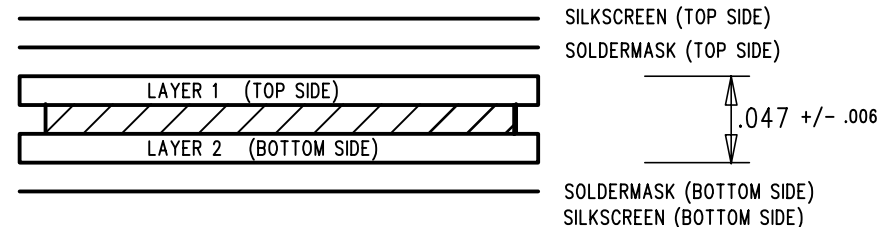
NOTES : (UNLESS SPECIFIED OTHERWISE.)

- 1) ALL DIMENSIONS ARE IN INCHES. TOLERANCE IS ± 0.005 CONFORMING TO IPC-A-600
- 2) HOLE SIZES ARE SPECIFIED IN THOUSANDTHS.
HOLE SIZES APPLY AFTER PLATING.
HOLE SIZE TOLERANCE TO BE ± 0.003 ,
UNLESS SPECIFIED OTHERWISE.
PLATING TO BE 0.0010 MINIMUM.
- 3) MATERIAL : FR-4-2 NATURAL EPOXY/FIBERGLASS
0.5 OZ. COPPER ALL LAYERS.
2 SIDES PLATED.
FINISHED THICKNESS : $0.047 \pm \frac{0.006}{-0.006}$

- 4) APPLY SOLDERMASK OVER BARE COPPER,
BOTH SIDES.
FINISH ALL EXPOSED COPPER SURFACES WITH
60/40% TIN/LEAD SOLDER, 100u" TO 1000u".
- 5) THE LOCATION OF THE MARKING SHOULD BE
ON THE SURFACE OF THE PCB, NOT THE EDGE.
- 6) APPLY SOLDERMASK TO COMPONENT SIDE
AND SOLDER SIDE, USING
☐ PC401 OR EQUIVALENT.
☒ LIQUID PHOTO IMAGEABLE.
☐ DRY FILM.
COLOR : GREEN.
USE SEPARATE FILM FOR COMPONENT SIDE
AND SOLDER SIDE SOLDERMASKS.
FABRICATOR SHALL MAKE NECESSARY
MODIFICATIONS TO SOLDERMASK PHOTOPLLOT FILES
FOR OPTIMAL SOLDERMASK COVERAGE BETWEEN
FINE PITCH COMPONENT LEADS.
- 7) APPLY LEGEND TO TOP SIDE
USING NON-CONDUCTIVE EPOXY INK.
COLOR : WHITE.
FABRICATOR SHALL MAKE NECESSARY
MODIFICATIONS TO LEGEND PHOTOPLLOT FILES
TO ENSURE NO LEGEND INK COVERS ANY COMPONENT
PAD OR VIA PAD.
- 8) PCB SHALL BE CLEAN AND FREE FROM DIRT,
OIL, FINGERPRINTS, CORROSION, AND ANY
OTHER FOREIGN MATERIAL.
- 9) MODIFIED PHOTOPLLOT FILES ARE TO BE RETURNED
BEFORE ORDER DELIVERED.
- 10) BOW AND TWIST NOT TO EXCEED 0.005" PER INCH.
- 11) ALL PRINTED CIRCUIT BOARD NETS SHALL BE 100%
ELECTRICALLY TESTED FOR OPENS AND SHORTS.
MARK TEXT VERIFICATION STAMP APPROXIMATELY
WHERE SHOWN, BOTTOM SIDE.



LAYER DETAIL
2 LAYERS



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APPROVALS		DATE	Järvevana tee 9 ARTEC DESIGN GROUP OÜ Tallinn, 11314 ESTONIA			
DRAWN	Elli Puusepp	09/19/2000	ZTAG PROGRAMMER Assembly Drawing Top			
CHECKED	Kaido Kevvai	09/19/2000				
PROJ MGR	ARTEC DG					
CLIENT		SIZE C	DRAWING NO: 10040306-01	SCALE 1 : 1	SHEET 1 OF 2	REVISION 1 6